(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 812 009 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
10.12.1997 Bulletin 1997/50

(21) Application number: **97303695.7**

(22) Date of filing: **02.06.1997**

(51) Int Cl.[6]: **H01L 21/265**, H01L 21/28, H01L 21/306, C03C 15/00, C23F 1/02

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: **03.06.1996 US 19120 P**

(71) Applicant: **TEXAS INSTRUMENTS INCORPORATED**
Dallas Texas 75265 (US)

(72) Inventors:
- **Kittl,Jorge Adrian**
  Plano Texas 75093 (US)
- **Misium ,George R.**
  Plano Texas 75074 (US)
- **Joyner,Keith A.**
  Richardson Texas 75081 (US)

(74) Representative: **Darby, David Thomas et al**
Abel & Imray
Northumberland House
303-306 High Holborn
London WC1V 7LH (GB)

(54) Improvements in or relating to semiconductor processing

(57) A method of forming silicided narrow (i.e., sub-0.25μm) polysilicon lines. A layer of titanium is deposited over a semiconductor body having polysilicon lines formed thereon. Either before or after the titanium deposition and before the react step, an implant is performed using a gas that will not poison the subsequent silicidation reaction. Exemplary gases include the noble element gases such as argon, krypton, xenon, and neon. The titanium is then reacted with the polysilicon lines to form titanium silicide. The gas implant causes the C49 grain size of the titanium silicide to be reduced, which makes the transformation to the C54 phase easier. Finally, an anneal is performed to transform the titanium silicide from the C49 phase to the C54 phase.

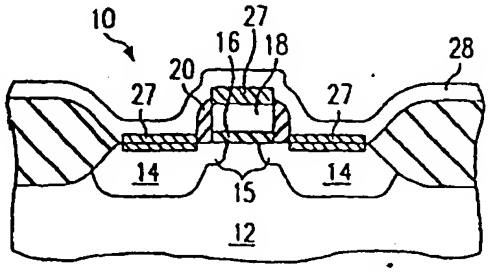

FIG. 1d

EP 0 812 009 A2

Description

FIELD OF THE INVENTION

This invention generally relates to semiconductor processing and more specifically to titanium silicide formation.

BACKGROUND OF THE INVENTION

As semiconductor technology progresses, the resistance of polysilicon lines used to form gates of MOSFET transistors becomes unacceptably high. As a result, silicide (such as titanium silicide) is commonly added to the polysilicon lines to reduce the resistance. In a self-aligned (salicide) process, a layer of titanium is deposited over the structure and reacted in a nitrogen ambient at temperatures of the order of 650-750°C. The titanium layer reacts with the silicon of the polysilicon lines and/or the source/drain regions of the transistors to form a titanium-silicide layer and with the nitrogen ambient to form a titanium nitride layer. The titanium nitride and any unreacted titanium are then removed. An anneal of the order of 800 - 900°C is then used to lower the sheet resistance and stabilize the titanium silicide phase (i.e., transform C49 phase titanium silicide to a lower resistance C54 phase).

The lower resistance C54 phase of titanium silicide is preferred over the higher resistance C49 phase. Unfortunately, as device geometries shrink, it becomes more and more difficult to transform the C49 phase to the C54 phase. Therefore, it is very difficult to form a low sheet resistance titanium salicide for sub-0.25μm CMOS technology. One proposed method to overcome this limitation is to use an arsenic implant prior to titanium deposition. The arsenic implant reduces the narrow linewidth effect. However, arsenic counterdopes the PMOS regions of CMOS devices if no masks are used for the implant step. Counterdoping is undesirable and induces problems such as higher silicide to source/drain contact resistance. Accordingly, there is a need to extend the usefulness of titanium-silicide to the sub-0.25μm technologies without the problems associated with an arsenic implant.

SUMMARY OF THE INVENTION

A method of forming silicided narrow polysilicon lines is disclosed herein. Polysilicon lines are formed on a semiconductor body and a layer of titanium is deposited over the structure. Either before the titanium deposition or after the titanium deposition and before the react step, an implant is performed using a gas that will not poison the subsequent silicidation reaction. Exemplary gases include the noble element gases such as argon, krypton, xenon, and neon. The titanium is then reacted with the polysilicon lines to form titanium silicide. Finally, an anneal is performed to transform the titanium silicide from the C49 phase to the C54 phase.

An advantage of the invention is providing a silicided narrow polysilicon line having low sheet resistance.

A further advantage of the invention is providing a silicided narrow polysilicon line having low sheet resistance that avoids the effects of chemical reactivity/doping associated with prior art techniques.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will now be further described, by way of example, with reference to the accompanying drawings in which:-

FIGs. 1a-e are cross-sectional diagrams illustrating a transistor undergoing a process according to a first embodiment of the invention;

FIG. 2 is a graph of dose/energy of a pre-amorphization implant according to the invention versus silicide sheet resistance of a 0.18μm linewidth;

FIG. 3 is a graph of dose/energy of a pre-amorphization implant according to the invention versus silicide sheet resistance of a 0.26μm linewidth; and

FIGs. 4a-e are cross-sectional diagrams illustrating a transistor undergoing a process according to a second embodiment of the invention

Corresponding numerals and symbols in the different figures refer to corresponding parts unless otherwise indicated.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

As device dimensions shrink, the sheet resistance of narrow silicided polysilicon lines after a titanium salicide process tends to increase as the linewidth decreases in the sub-micron range. This is known as the narrow linewidth effect. Rapid thermal processing solves the narrow width effect problem in devices having minimum geometries greater than 0.25 μm. However, device geometries are now shrinking to below 0.25 μm. The invention will be described in conjunction with a MOSFET process flow. However, it is applicable to narrow titanium silicided lines in general. The invention utilizes a pre-amorphization implant either before titanium deposition or after deposition and before react using a gas implant that does not poison the silicidation process. The gas, for example one of the noble elements, does not act as a dopant and therefore no masking steps are necessary. In addition, there is no chemical reactivity between the gas and the salicide. The pre-amorphization implant reduces the narrow linewidth effect for device geometries smaller than 0.25 μm.

A more detailed description of a method of forming

narrow silicided polysilicon lines according to a first embodiment of the invention will now be discussed with reference to FIGs. 1a-1e. FIG. 1a is a cross-section of a transistor 10 processed through source/drain anneal. Transistor 10 is formed in a semiconductor body 12 and includes source/drain regions 14, lightly-doped drain extensions 15, a gate oxide 16 and polysilicon gate electrode 18. Sidewall dielectric 20 is located on the sidewalls of gate oxide 16 and polysilicon gate electrode 18. Polysilicon gate electrode 18 is actually a long narrow polysilicon line that forms the gate electrode of several transistors. As device dimensions shrink, the width of polysilicon gate electrode 18 shrinks below 0.25μm.

Referring to FIG. 1b, a blanket implant is performed next. The implant is of an inert gas that does not poison the subsequent silicide reaction. Examples of gases that may be used include the noble elements such as Argon, Xenon, Neon, and Krypton. Silicon should not be used because it causes interstitials. Oxygen poisons the silicidation reaction. Hydrogen and helium are probably too light to be effective. Using an inert gas that does not poison the silicide reaction instead of a dopant avoids both counterdoping the PMOS regions of a CMOS device and the masking requirement used to avoid counterdoping the PMOS regions.

The implant amorphizes the surface of the polysilicon gate electrode 18 and the source/drain regions 14. The dose of the implant is of the order of 3E14/cm^2 and greater. However, the dose should not be so high as to cause knock-on or ion-mixing from the screen layer 24 that can poison the subsequent silicide reaction with oxygen. The energy of the implant is chosen such that the surface is amorphized to a depth less than the source/drain junction region. This may typically be of the order of 1/2 the junction depth of the source/drain regions 14. If the amorphized region extends past the junction depth, the implant can interfere with transistor operation causing increased leakage. Preferably, the depth of the amorphized region is matched to the amount of the source/drain regions 14 and polysilicon gate electrode 18 that will be consumed during the subsequent silicide formation. Thus, the optimum dose and energy will vary depending on the element implanted, the design parameters of the transistor 10 and the thickness of screen oxide 24. As an example, for an argon pre-amorphization implant through a 100 Angstrom screen oxide to form a 0.18 μm gate electrode, appropriate energies include approximately 18-20 keV and above with a dose of the order of 5E14.

After the pre-amorphization implant of the inert gas, the screen oxide 24 is removed and standard clean-up steps may be performed. If desired, screen oxide 24 may be removed prior to the pre-amorphization implant. In that case, the surface of the structure may also undergo standard clean-up processes prior to the pre-amorphization implant.

Referring to FIG. 1c, a layer of titanium 26 is deposited over the structure. The thickness of titanium layer 26 is chosen for conventional reasons (i.e., thickness desired for resulting silicide layer, device design parameters, etc.). For example, titanium layer 26 may be of the order of 300 Angstroms thick. The titanium layer 26 is then reacted with the silicon in source/drain regions 14 and polysilicon gate electrode 18 in a nitrogen ambient to form a silicide layer 27 as shown in FIG. 1d. For example, a rapid thermal process of the order 700 °C for of the order of 60 seconds may be used. However, an appropriate furnace treatment may also be used. This react process creates a silicide in a mostly high resistivity phase, known as C49. The pre-amorphization implant of the inert gas causes the C49 grain size to be smaller than it otherwise would be. The C49 grain size created with the pre-amorphization implant is smaller than the polysilicon gate electrode width. Having a C49 grain size smaller than the linewidth makes it easier to transform a higher percentage of silicide layer 27 from the C49 phase to a lower resistivity C54 phase during the subsequent anneal. When the polysilicon linewidth is less than the C49 grain size, the thermal budget required to transform the C49 phase to the C54 phase increases dramatically leading to agglomeration. By optimizing the pre-amorphization implant, RTP react process and the subsequent RTP anneal process, a C49 grain size of the order of 0.07 μm can be achieved.

In places where there is no silicon for the titanium layer 26 to react with, titanium nitride 28 is formed. There may also be some unreacted titanium left. As shown in FIG. 1e, the titanium nitride 28 and any unreacted titanium are then removed. Finally, a silicide anneal is performed to transform the titanium-silicide of silicide layer 27 from a higher resistivity C49 phase to a lower resistivity C54 phase. This anneal may be performed either as a rapid thermal process (RTP) or in a furnace. For example, an RTP process at a temperature of the order of 850°C for of the order of 30 sec. may be used.

FIGs. 2-3 illustrate the effect of an Argon pre-amorphization implant on a titanium silicided NMOS gate sheet resistance. FIG. 2 shows the effect of various dose/energy splits on sheet resistance for a 0.18μm gate. Argon is implanted prior to titanium deposition through a 100 Angstrom screen oxide. A 300 Angstrom layer of titanium is deposited, reacted and annealed. At energies of the order of 20 keV and above and a dose of 5E14/cm^2, significant reduction in the sheet resistance of the silicided gate can be observed. FIG. 3 shows the results of a similar process for a 0.26 μm gate. Here, significant reduction in the sheet resistance can be observed for energies as low as 15 keV. A marked decrease in resistance variability can be observed in increasing the dose form 3E14/cm^2 to 5E14/cm^2 at 15 keV.

A method of forming narrow silicided polysilicon lines according to a second embodiment of the invention will now be discussed with reference to FIGs. 4a-4d. FIG. 4a is a cross-section of a transistor 10 processed through source/drain anneal. As in FIG. 1a, transistor

10 is formed in a semiconductor body 12 and includes source/drain regions 14, lightly-doped drain extensions 15, a gate oxide 16 and polysilicon gate electrode 18. Sidewall dielectric 20 is located on the sidewalls of gate oxide 16 and polysilicon gate electrode 18. Polysilicon gate electrode 18 is actually a long narrow polysilicon line that forms the gate electrode of several transistors. As device dimensions shrink, the width of polysilicon gate electrode 18 shrinks below 0.25μm.

Referring to FIG. 4b, screen oxide 24 is removed. Standard cleanup processes may then be performed. At this point, a layer of titanium 26 is deposited. The thickness of titanium layer 26 is chosen for conventional reasons (i.e., thickness desired for resulting silicide layer, device design parameters, etc.). For example, titanium layer 26 may be of the order of 300 Angstroms thick.

Prior to reacting titanium layer 26 with the silicon in polysilicon gate 18 and source/drain regions 14, a pre-amorphization implant is performed, as shown in Figure 4c. As in the first embodiment, the implant is of an inert gas that does not poison the subsequent silicide reaction. Examples of gases that may be used include the noble elements such as Argon, Xenon, Neon, and Krypton. Using an inert gas that does not poison the silicide reaction instead of a dopant avoids both counterdoping the PMOS regions of a CMOS device and the masking requirement used to avoid counterdoping the PMOS regions.

The implant amorphizes the surface of the polysilicon gate electrode 18 and the source/drain regions 14 through the titanium layer 26. The dose of the implant is of the order of $3E14/cm^2$ and greater. The energy of the implant is adjusted to account for the overlying titanium latyer 26 such that the surface of the silicon is amorphized to a depth less than the source/drain junction region. The titanium/silicon interface needs to be amorphous on the silicon side. Thus, the depth may typically be of the order of 1/2 the junction depth of the source/drain regions 14. If the amorphized region extends past the junction depth, the implant can interfere with transistor operation causing increased leakage. Preferably, the depth of the amorphized region is matched to the amount of the source/drain regions 14 and polysilicon gate electrode 18 that will be consumed during the subsequent silicide formation. Thus, the optimum dose and energy will vary depending on the element implanted, the design parameters of the transistor 10, and the thickness of titanium layer 26. As an example, for an argon pre-amorphization implant, a 20 KeV Ar at a dose of $3e14\ cm^{-2}$ may be used.

Referring to FIG. 4d, the titanium layer 26 is then reacted with the silicon in source/drain regions 14 and polysilicon gate electrode 18 in a nitrogen ambient to form a silicide layer 27. For example, a rapid thermal process of the order 700 °C for of the order of 60 seconds may be used. However, an appropriate furnace treatment may also be used. This react process creates a silicide in a mostly high resistivity phase, known as C49. The pre-amorphization implant of the inert gas causes the C49 grain size to be smaller than it otherwise would be. The C49 grain size created with the pre-amorphization implant is smaller than the polysilicon gate electrode width. Having a C49 grain size smaller than the linewidth makes it easier to transform a higher percentage of silicide layer 27 from the C49 phase to a lower resistivity C54 phase during the subsequent anneal. When the polysilicon linewidth is less than the C49 grain size, the thermal budget required to transform the C49 phase to the C54 phase increases dramatically leading to agglomeration. By optimizing the pre-amorphization implant, RTP react process and the subsequent RTP anneal process, a C49 grain size of the order of 0.07 μm can be achieved.

In places where there is no silicon for the titanium layer 26 to react with, titanium nitride 28 is formed. There may also be some unreacted titanium left. As shown in FIG. 4e, the titanium nitride 28 and unreacted titanium 26 are then removed. Finally, a silicide anneal is performed to transform the titanium-silicide of silicide layer 27 from a higher resistivity C49 phase to a lower resistivity C54 phase. This anneal may be performed either as a rapid thermal process (RTP) or in a furnace. For example, an RTP process at a temperature of the order of 850°C for of the order of 30 sec. may be used.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description.

Claims

1. A method of forming a silicided polysilicon line on a semiconductor body comprising the steps of:

   forming a polysilicon line on said semiconductor body;
   implanting a gas that does not poison a subsequent silicidation reaction into said polysilicon line and said semiconductor body;
   depositing a layer of titanium over said polysilicon line;
   reacting said layer of titanium with said polysilicon layer to form a silicide layer such that said implanted gas causes a grain size of said silicide layer to be reduced; and
   annealing said silicide layer to transform the silicide layer from a higher resistivity phase to a lower resistivity phase.

2. The method of Claim 1, wherein said step of implanting said gas comprises implanting a gas comprising a noble element.

3. The method of Claim 1 or Claim 2, wherein said step of implanting said gas comprises implanting said gas at a dose of the order of 3E14/cm^2 or greater.

4. The method of any preceding Claim, wherein said step of implanting said gas comprises implatning said gas after said step of depositing a layer of titanium.

5. The method of any preceding Claim further comprising the step of:
forming a source/drain region after said step of forming said polysilicon line and prior to said steps of implanting a gas and depositing a layer of titanium.

6. The method of any preceding claim further comprising;
performing the step of implanting said gas at an energy chosen such that said gas is implanted to less than one half of a junction depth of said source/drain region.

7. The method of any of claims 1 to 5 further comprising performing the step of implanting said gas until said gas is implanted to a depth approximately equal to a depth of a portion of said polysilicon line that is consumed by said reacting step.

8. The method of any of Claims 1 to 5 further comprising performing the step of implanting said gas until said gas is implanted to a depth less than a depth of a portion of said polysilicon line that is consumed by said reacting step.

9. The method of any preceding Claim further comprising performing the step of implanting said gas such that said gas is implanted at a dose sufficient to amorphize the surface of said polysilicon line.

10. The method of any preceding Claim, wherein said reacting step comprises a rapid thermal anneal in a nitrogen ambient at a temperature of the order of 700°C.

11. The method of Claim 10, wherein the reacting step further comprises the step of removing any unreacted portions of said titanium layer and a layer of titanium nitride formed during said reacting step prior to said annealing step.

12. The method of Claim 10 or Claim 11 further comprising performing said annealing step at a temperature in the range of 700-950°C.

13. A method of forming a silicided polysilicon line on a semiconductor body comprising the steps of:
forming a polysilicon line on said semiconductor body;
forming a source/drain region adjacent said polysilicon line in said semiconductor body;
implanting a noble element using a blanket implant to amorphize a surface of said polysilicon line;
depositing a layer of titanium over said semiconductor body including said polysilicon line and said source/drain region;
reacting said layer of titanium with said polysilicon line and said source/drain region to form a silicide layer such that said silicide layer has a reduced grain size due to said implanting step; and
annealing said silicide layer to transform said silicide layer from a higher resistivity phase to a lower resistivity phase.

14. The method of Claim 13, wherein said step of implanting said noble element comprises implanting argon.

15. The method of Claim 13, wherein said step of implanting a noble element comprises implanting xenon.

16. The method of any of Claims 13 to 15 further comprising implanting said noble element at a dose of the order of 3E14/cm^2 or greater.

17. The method of any of Claims 13 to 16 further comprising performing said step of implanting a noble element at an energy chosen such that said noble element is implanted to less than one half of a junction depth of said source/drain region.

18. The method of any of Claims 13 to 16 further comprising performing said step of implanting said noble element such that said noble element is implanted to a depth approximately equal to or less than a depth of a portion of said polysilicon line that is consumed by said reacting step.

19. The method of any of Claims 13 to 16, wherein said reacting step comprises a rapid thermal anneal in a nitrogen ambient at a temperature of the order of 700°C.

20. The method of Claim 19 further comprising the step of removing any unreacted portions of said titanium layer and a layer of titanium nitride formed during said reacting step prior to said annealing step.

21. The method of Claim 19 or Claim 20 further comprising performing said annealing step at a temperature in the range of 700-950°C.

22. The method of any of Claims 13 to 21, wherein the step of forming said polysilicon line comprises forming a polysilicon line having a linewidth of less than 0.25μm.

FIG. 1a

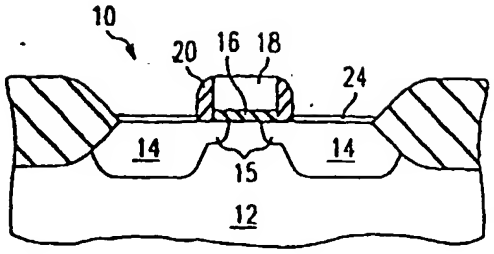

FIG. 1b

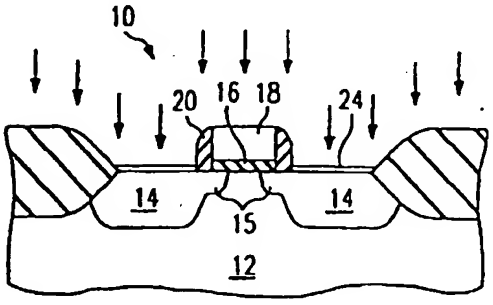

FIG. 1c

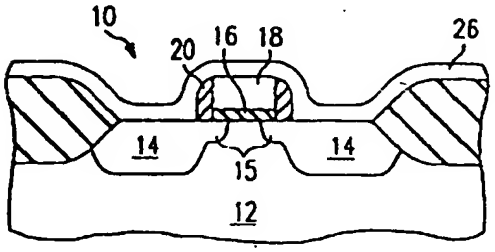

FIG. 1d

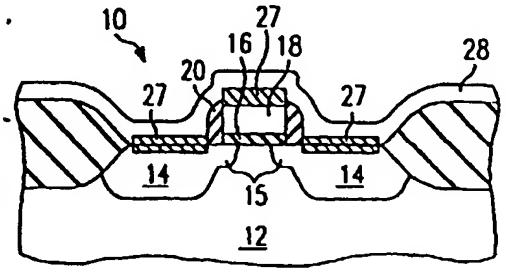

FIG. 1e

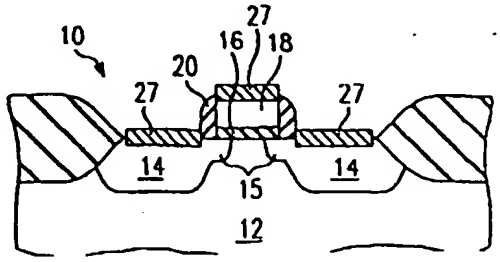

FIG. 2

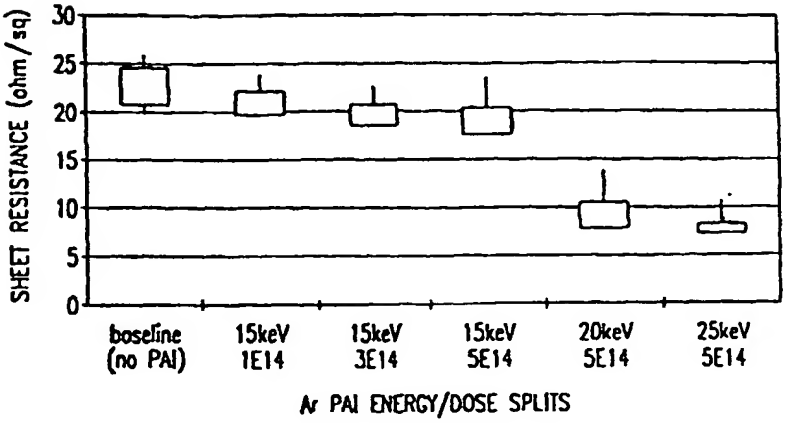
SHEET RESISTANCE (ohm/sq)
30
25
20
15
10
5
0
baseline (no PAI)
15keV 1E14
15keV 3E14
15keV 5E14
20keV 5E14
25keV 5E14
Ar PAI ENERGY/DOSE SPLITS

FIG. 3

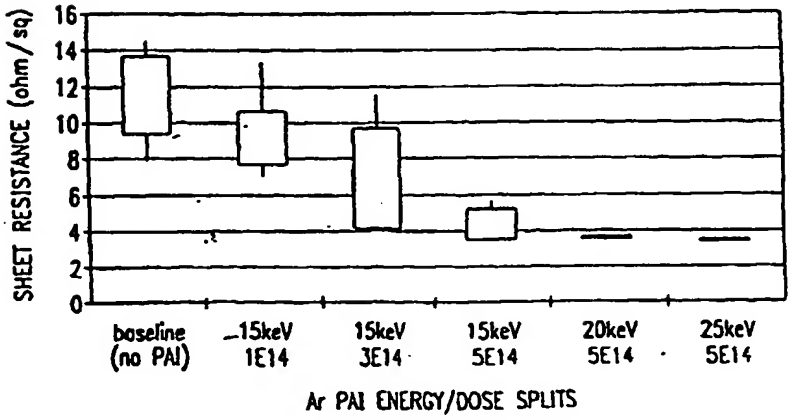
SHEET RESISTANCE (ohm/sq)
16
14
12
10
8
6
4
2
0
baseline (no PAI)
15keV 1E14
15keV 3E14
15keV 5E14
20keV 5E14
25keV 5E14
Ar PAI ENERGY/DOSE SPLITS

FIG. 4a

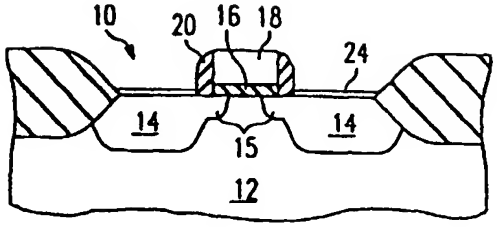

FIG. 4b

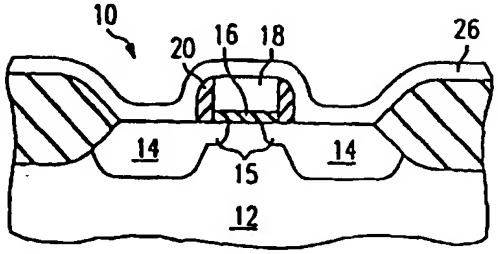

FIG. 4c

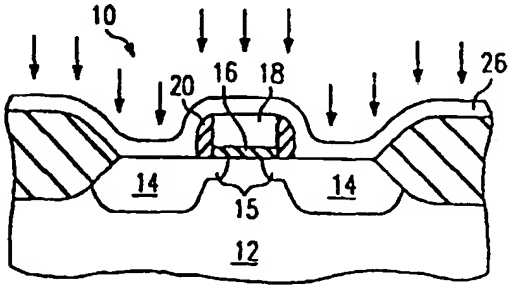

FIG. 4d

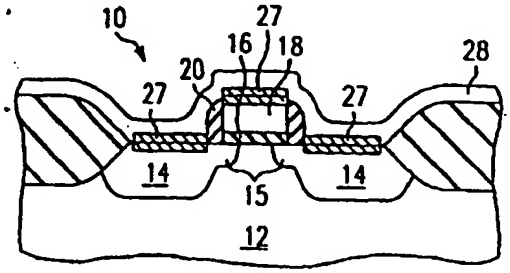

FIG. 4e